

I claim:

1. A process of adapting a synthesized scan-BIST architecture for low power operation comprising:

A. partitioning the scan path of said scan BIST architecture into multiple separate scan path sections, each section having a scan input and a scan output;

B. forming a connection between the scan inputs of each scan path section;

C. forming a selective connection between the scan outputs of each scan path section;

D. providing a scan control circuit having separate scan control outputs; and

E. forming separate connections between each of said separate control outputs and one of said scan path sections.

2. A scan BIST test circuit, within an integrated circuit, comprising:

A. a plurality of scan paths each having a scan input, scan output, and a control input;

B. a generator circuit having a control input and a stimulus data output;

C. a compactor circuit having a control input and a response data input;

D. a control circuit providing control output to said control inputs of said scan path, generator circuit, and compactor circuit,;

E. a first connection formed between said stimulus data output of said generator circuit and all of said scan inputs of said plurality of scan paths; and

F. a second connection selectively formed between said response data input of said compactor circuit and ones of said scan outputs of said plurality of scan paths.

3. A scan BIST test configuration of a circuit, within an integrated circuit, comprising:

- A. a scan path having a first control input;
- B. a generator having a second control input;
- C. a compactor having a third control input;
- D. a first controller having first control output;
- E. a second controller having a fourth control input and second control output;
- F. a connection between said first control output and said second, third, and fourth control inputs; and
- G. a connection between said second control output and said first control input.

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